

**WHAT IS CLAIMED IS:**

1 1. A method comprising the steps of:  
2       when in a first mode of operation, utilizing a first output to provide a first data lane enable  
3       for facilitating access of a portion of a first memory storage location associated with  
4       a first memory address; and  
5       when in a second mode of operation, utilizing the first output to provide an address bit of a  
6       second memory address for facilitating designation of a second memory storage  
7       location.

1 2. The method of claim 1 wherein:  
2       the first data lane enable facilitates accessing a byte of data associated with the first memory  
3       address when in the first mode of operation; and  
4       the second memory address accesses a byte wide memory.

1 3. The method of claim 1 wherein:  
2       the first data lane enable facilitates accessing a byte of data associated with the first memory  
3       address when in the first mode of operation; and  
4       the second memory address accesses a word wide memory.

1 4. The method of claim 3 wherein the number of bits associated with the word wide memory is  
2       greater than 8.

1 5. The method of claim 1 wherein:  
2       the first and second modes of operation utilize the first output to access a device external a  
3       device that includes the first output.

- 1 6. The method of claim 5 further comprising the step of:  
2 when in a third mode of operation, utilizing the first output to provide information about a  
3 memory access internal to the device that includes the first output.
- 1 7. The method of claim 1, wherein:  
2 the address bit is an additional address bit used to extend an address range when a memory  
3 having a width less than a word width is being accessed.
- 1 8. The method of claim 1, further comprising the step of:  
2 determining a mode of operation to be one of the first mode of operation and the second  
3 mode of operation.
- 1 9. The method of claim 8, wherein:  
2 the step of determining the mode of operation is based upon a register value associated with  
3 a specific chip select.
- 1 10. The method of claim 1 further comprising:  
2 when in the first mode of operation, utilizing a second output to provide an address bit of the  
3 first memory address for facilitating designation of the first memory storage location;  
4 and  
5 when in the second mode of operation, utilizing the second output to provide a second data  
6 lane enable for facilitating access of a portion of the second memory storage location  
7 associated with the second memory address.

1 11. A method of providing data to a set of pins of a device, the method comprising the steps of:  
2 during a first mode of operation, multiplexing a first set of data onto the set of pins to allow  
3 the set of pins to provide data representing two least significant bits of a first address,  
4 a most significant bit of the first address, and a lane enable;  
5 during a second mode of operation, multiplexing a second set of data onto the set of pins to  
6 allow the set of pins to provide data representing one least significant bit of a second  
7 address, a most significant bit of the second address, and two lane enables; and  
8 during a third mode of operation, multiplexing a third set of data onto the set of pins to allow  
9 the set of pins to provide four lane enables.

1 12. The method of claim 11, wherein the first, second and third sets of data facilitate an external  
2 memory access, wherein the external memory access is external relative to the device.

1 13. The method of claim 12, further comprising the step of:  
2 during a fourth mode of operation multiplexing a fourth set of data onto the set of pins to  
3 allow the set of pins to provide information relating to an internal memory access.

1 14. The method of claim 11 further comprising the step of:  
2 determining the mode of operation is based upon a chip select indicator.

- 1 15. An apparatus comprising:  
2 a set of address nodes to provide address data for address location A(n) through A(2), where  
3 A(n) represents a most significant bit for at least a first mode of operation;  
4 a first output node to provide one of an address data for address location A(1) and a data lane  
5 enable signal based upon a mode of operation;  
6 a second output node to provide one of an address data for address location A(0) and a data  
7 lane enable signal based upon the mode of operation; and  
8 a third output node to provide one of an address data for address location A(n+1) and a data  
9 lane enable signal based upon the mode of operation.

- 1 16. An apparatus comprising:  
2 a first register having an output to indicate one of a first mode of operation and a second  
3 mode of operation;  
4 an address control portion having an input coupled to the output of the first register, and an  
5 output to indicate a value of an address bit when in the first mode of operation;  
6 a first data lane enable control portion having an input coupled to the output of the first  
7 register, and an output to indicate a first data lane enable value when in the second  
8 mode of operation; and  
9 an output pin coupled to the output of the address control portion and the output of the first  
10 data lane enable control portion.
- 1 17. The apparatus of claim 16 wherein a multiplexor having a control input coupled to the output of  
2 the first register, a first data input coupled to the address control pin, a second data input  
3 coupled to the first data lane enable, and an output coupled to the output pin.
- 1 18. The apparatus of claim 16, wherein the first register is associated with one of a plurality of chip  
2 selects.

1 19. A system comprising:  
2 a processing module coupled to a set of outputs; and  
3 memory operably coupled to the processing module, wherein the memory stores operational  
4 instructions that cause the processing module to:  
5 utilize a first output to provide a first data lane enable to facilitate accessing of a  
6 portion of a first memory storage location associated with a first memory  
7 address when in a first mode of operation; and  
8 utilize the first output to provide an address bit of a second memory address to  
9 facilitate designation of a second memory storage location when in a second  
10 mode of operation.

1 20. The system of claim 19 further comprising:  
2 operational instructions that cause the processing module to:  
3 when in a third mode of operation, utilize the first output to provide information  
4 about a memory access internal to the device.

- 1 21. A method of operating a microcomputer, comprising the steps of:
- 2 when the microcomputer is in a first mode of operation, utilizing a first output of a
- 3 microcomputer to provide a first data lane enable for facilitating access of a portion
- 4 of a first memory storage location associated with a first memory address; and
- 5 when the microcomputer is in a second mode of operation, utilizing the first output of the
- 6 microcomputer to provide an address bit of a second memory address for facilitating
- 7 designation of a second memory storage location.